REMARKS

This is intended as a full and complete response to the Office Action dated April 23, 2007, having an extended period for response set to expire on August 23, 2007. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-22 are pending in the application. Claims 1-22 remain pending following entry of this response. Claim 5 has been amended. Applicants submit that the amendments do not introduce new matter.

Claim Rejections - 35 U.S.C. § 103

Claims 1-3, 10, 17 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Bando* (U.S. Publication 2002/0145930) and in view of *Nakamura* (U.S. Patent No. 6,898,683).

Claims 4-7, 8-9, 11-16 and 18-20 are rejected under 3S U.S.C. 103(a) as being unpatentable over *Bando*, *Nakamura* as applied to claims 1, 3, 10, 17 and further in view of *Kirihata et al.* (U.S. Patent No. 6,404,689, hereinafter, "*Kirihata*"). The Examiner takes the position that while *Bando* does not expressly disclose the claims' aspect of a command buffer device receiving a multi-bit status containing the period and type of a critical operating state of a control device, *Nakamura*, however, discloses a memory control device having such circuitry. Therefore, the Examiner concludes, it would have been obvious to one of ordinary skill in the art at the time of invention to include a critical status signal as suggested by Nakamura in a system such as *Bando*.

Applicants respectfully traverse this rejection.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there

must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejection fails to establish at least the third criteria.

In regards to claim 1, the control device controls and initiates operations of the memory cells in response to decoded external commands. The decoded external commands are supplied by the command buffer device in response to a multi-bit status signal, supplied by the control device, which indicates the critical operating state period and the type of critical operating state. If the multi-bit status signal indicates that the memory is in a critical operation state, the command buffer device will prevent execution of the next operation stored in the buffer. Conversely, once the multi-bit status indicates that the memory is no longer in a critical operation state, the command buffer device will execute the next operation stored in the buffer. (See paragraph [0025] of the specification).

In contrast, Nakamura discloses a clock input buffer that generates multiple clock signals, where each clock is routed to different parts of logic in the circuit. (See *Nakamura*, Figure 2). The purpose of having multiple clocks is to allow the ability to disable logic not in use by turning off the clock that feeds that logic, thus reducing unnecessary power consumption. (See *Nakamura*, col 6, lines 32-46, Figures 2 and 8).

The Examiner erroneously equates the multiple clock signals with the multi-bit status signal disclosed in the present invention. The functionality of the clock is not the same as the multi-bit status signal of the present invention. While it is true that the clock and the multi-bit status signals can be reactive to similar situations, such as self-refresh mode, the behavior is fundamentally different. The multi-bit status signal is encoded with information regarding the period and type of the critical operating state of the control device. It is then decoded by the command buffer to determine the start of execution of the next operation. On the other hand, the clock, by its nature, simply does not have the capability to contain such encoded information (at least as it is disclosed in *Nakamura*). Therefore, the clock cannot assist the command buffer to determine the

start of execution of the next transaction. Instead, the clock (or lack thereof) simply disables that logic all together.

Moreover, the Examiner attempts to equate the combination of CLK2x and CLK2z of Figure 5 in *Nakamura*, as being a multi-bit status signal. The desired effect of having the two clocks per buffer circuit is to operate the gate electrode of the transfer gates in the buffer circuits (See *Nakamura*, col. 7, lines 58-63, Figure 5), not to somehow create an encoding similar to the multi-bit status signal of the present invention. Thus, *Nakamura* does not teach the multi-bit status signal as recited in the present claims.

Examiner has applied the same argument (i.e., that the multiple clock signals disclosed in Nakamura are equivalent to the multi-bit status signal of the present invention) with respect to independent claims 10, 17, 21 and 22. The rejection of claim 1 has been overcome for the reasons given above. Accordingly, the remaining independent claims are also believed to be allowable.

Furthermore, Claims 2-9 depend from claim 1, claims 11-16 depend from claim 10, claims 18-20 depend from claim 17. The rejections of claims 1, 10, 17, 21 and 22 have been overcome for the reasons given above. Accordingly, their respective dependent claims are also believed to be allowable.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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